REMARKS

The Applicants respectfully request reconsideration and allowance of claims 1-18 in view of the following arguments.

INTERVIEW SUMMARY

The Applicants appreciate the telephone interview conducted January 11, 2005, between Examiner Sharon, his supervisor, and the undersigned attorney. In the interview, the undersigned attorney summarized the arguments presented below and emphasized the fundamental distinctions between the Teene patent (U.S. Patent No. 6,272,668, hereinafter referred to as "Teene") and Applicants' claims. The general difference between Teene and Applicants' claims were discussed as well as some of the particular differences between the static timing analysis of Applicants' claims and the analysis conducted in Teene. Specifically, Teene's use of automatic analysis in post-layout circuit design was discussed in relation to Applicants' static timing analysis techniques. No agreement was reached as to the allowability of the claims.

CLAIMS 1-18 ARE NOT ANTICIPATED BY THE CITED PRIOR ART

The Examiner rejected claims 1-18 under 35 U.S.C. § 102(e) as being anticipated by Teene. The Applicants respectfully submit that the claims are not anticipated by this reference.

The Teene Patent

Teene discloses a system that relies on "statistical, historical information" to determine the timing of an application specific integrated circuit (ASIC) rather than relying on static timing analysis tools for the ASIC design (col. 6, lines 18-24). In other words, although the Teene

PAGE 3/7 * RCVD AT 2/15/2005 2:51:56 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:512 327 2665 * DURATION (mm-ss):02-34

patent is directed to a system for improving timing performance of a standard cell ASIC layout, Teene improves the timing performance by testing post-layout timing performance to determine whether to swap circuit cells of an ASIC layout (col. 5, lines 17-21).

The Teene Patent Fails to Teach Each Element Required in the Respective Claims

Applicants' independent claim 1 is directed to a method for analyzing an electronic circuit and requiring the following events:

(a) replacing at least one timing determinant block in a first functional component of the circuit with a timing element set;
(b) performing a circuit simulation for a cross-section of the first functional component to determine timing characteristics associated with each replaced timing determinant block of the first functional component;
(c) attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block, thereby creating a timing model for the first functional component; and
(d) performing a static timing analysis for the circuit utilizing the timing model for the first functional component.

The Examiner appears to liken Teene's swapping of standard cell components with other functionally equivalent standard cell circuit components at col. 11, lines 63-67 to "replacing at least one timing determinant block in a first functional component of the circuit with a timing element set" as required in Applicants' claim 1 at element (a). However, Teene's swapping of standard cell components for functionally equivalent standard cell circuit components is different than replacing a timing determinant block with a timing element set because the timing determinant block is completely removed from the timing model that is eventually created according to the present invention, and not swapped for another timing determinant block. Teene's cell swapping is merely to improve the timing slack value on each timing arc in a sorted list of timing arcs (col. 11, lines 66-67). On the other hand, Applicants claim replacing a timing

PAGE 4/7 * RCVD AT 2/15/2005 2:51:56 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729308 * CSID:512 327 2665 * DURATION (mm-ss):02-34

determinant block with a timing element set. The timing element set of Applicants' claims reduces the processing that would otherwise be required to perform a static timing analysis of an electronic circuit when compared to using a new or swapped cell circuit component as per Teene. In other words, Teene swaps cells to find the "optimum timing slack value" (col. 12, line 3) rather than replace a cell with a timing element set to create a timing model for a static timing analysis.

The Examiner also appears to liken Teene's computing of "temporary variables" for use in the analysis of standard cell circuit components at col. 15, lines 37-43 to "performing a circuit simulation for a cross-section of the first functional component" as required in Applicants' claim 1, element (b). Applicants' note that the circuit simulation of element (b) is "to determine timing characteristics associated with each replaced timing determinant block." However, as discussed above, Teene swaps cells to find the optimum timing slack value. This computing of temporary slack values cannot be considered to be performing a circuit simulation for a cross-section of the first functional component because Teene's computing of the temporary variables is not simulation of a cross section at all.

Also in the Office Action, the Examiner refers to the "two temporary values used to evaluate the possible improvement in timing slack caused by swapping the equivalent cell for the current cell" at col. 16, lines 5-7 in Teene as disclosing element (c) of Applicants' claim 1. This disclosure cannot teach "attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block" as required in Applicants' claim 1 at element (c) because in Teene, no timing

PAGE 5/7 * RCVD AT 2/15/2005 2:51:56 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:512 327 2665 * DURATION (mm-ss):02-34

determinant block is replaced by a timing element set and thus, no timing characteristic in Teene can be attached to any timing element set.

Regarding element (d) of Applicants' claim 1, the Examiner points to col. 16, lines 7-15 in Teene in an attempt to show performing a static timing analysis for the circuit. However, nothing in Teene discloses performing a static timing analysis utilizing a timing model that includes a timing element set that replaced a timing determinant block as required by element (d) of Applicants' claim 1. In addition, Teene discourages the use of static timing analysis tools when, for example, Teene states that prior art "reliance on static timing analysis renders the method [of automating ASIC layouts] less useful to ASIC designs" (Teene, col. 3, lines 18-65 with specific attention to lines 57-59).

For the above reasons the Teene reference fails to teach or suggest any of the four elements required in claim 1. Thus, Applicants urge the Examiner to withdraw the § 102 rejection of independent claim 1 as being anticipated by Teene. Likewise, claims 2-7 depend from claim 1 and the limitations of claim 1 apply to claims 2-7. Thus, the Examiner is urged to withdraw the § 102 rejection of claims 2-7.

Regarding, Applicants' independent claims 8 and 14 with their respective dependent claims, Applicants respectfully submit that these claims require similar limitations as found in claims 1 through 7. Thus, the arguments presented above with respect to claim 1 apply with equal force to independent claims 8 and 14 and their respective dependent claims.

PAGE 6/7 * RCVD AT 2/15/2005 2:51:56 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:512 327 2665 * DURATION (mm-ss):02-34

CONCLUSION

For all of the above reasons, the Applicants respectfully request reconsideration and allowance of claims 1-18.

If any issue remains as to the allowability of these claims, or if a conference might expedite allowance of the claims, the Examiner is asked to telephone the undersigned attorney prior to issuing a further action in this case.

Respectfully submitted,

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 703-872-9306) on February 15, 2005.

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PAGE 7/7 * RCVD AT 2/15/2005 2:51:56 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:512 327 2665 * DURATION (mm-ss):02-34